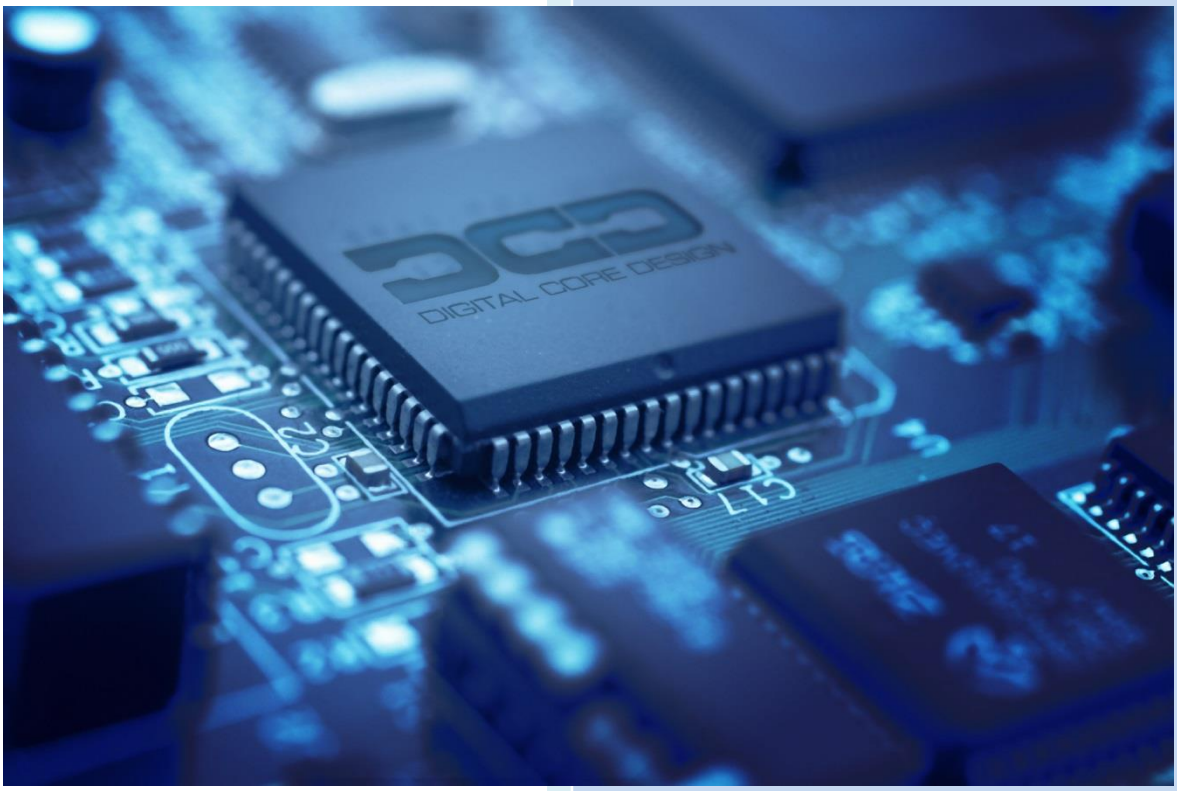
DIGITAL CORE DESIGN

2016

DoCD IP Core



68HCXX - DCD on Chip Debug System v. 3.01

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DCD's on-chip Debug System (DoCD™) prominently cuts debugging time. Integrating DCD IP Cores with a Hardware Assisted Debugger and Debug IP Core, provides a powerful SoC development tool, with advanced features. The DoCD™ system consists of three major blocks:

- Debug IP Core
- Hardware Assisted Debugger
- Debug Software

The Debug IP Core block is a **real-time hardware debugger**, which provides an access to all chip registers, memories and peripherals, connected to DCD's IP Core (Dx8051/Dx80390 /DRPIC/ DFPIC/Dx6811) and controls CPU work by **non-intrusive** method. A high-performance Hardware Assisted Debugger (**USB-xTAG**) is connected to the target system containing the DCD's core either in FPGA or ASIC. The Hardware Assisted Debugger manages communication between the Debug IP Core inside silicon using DTAG, TTAG, or JTAG protocol, and Debug Software using USB port.

HAD

Hardware Assisted Debugger (HAD) is a hardware adapter, that manages communication between the Debug IP Core inside silicon and a USB port of the host PC running DoCD™ Debug Software.

SYSTEM FEATURES

- SOFTWARE BREAKPOINTS:

An unlimited number of software breakpoints can be set anywhere in the physical address space of the processor (in Program Memory space, RAM and SFRs). If at least one software breakpoint is set, program is executed in automatic step by step mode, with checking, if certain breakpoint condition is met. Program execution is halted, when breakpoint condition is already met, and its execution can be resumed at any time in any appropriate mode.

- HARDWARE BREAKPOINTS:

The number of hardware breakpoints is limited to four in different address spaces. Like software breakpoints, hardware execution breakpoints can be set in Program Memory space, RAM and SFRs. Like their software counter-parts, they stop program execution just prior an instruction is being executed. The difference is in the method of program execution. In this case program is run with full clock speed (in real-time) and processor is halted, when hardware signalizes real breakpoint condition.

- MIXED MODE BREAKPOINTS:

Mixed breakpoint mode is also allowed and it means, that software and hardware breakpoints are mixed in the system. This gives you the flexibility in the debugging - for example, two different break conditions can be set at the same address space, by using software and hardware breakpoints. In each breakpoint mode, halt means: CPU is halted and instructions are no longer being fetched, all peripherals are running and are not affected by halt.

- SCALED SOLUTION:

Due to the fact, that many SoC designs have both power and gate limitations, DCD provides a scaled solution. Debug extensions can be scaled to control gate counts. The benefit is fewer gates - for lower use of power and core size, while maintaining excellent debug abilities

DEBUG IP CORE

The Debug IP Core can be provided as VHDL or Verilog source code, as well as CPLD/FPGA EDIF Netlist, depending on the customer requirements. Due to the fact, that many SoC designs have both power and area limitations, DoCD™ provides scaled solution. Debug IP Core can be scaled to control gate count. The benefit is fewer gates – for lower use of power and core size, while maintaining excellent debug abilities. Typically, all the features are utilized in pre-silicon debug (i.e. hardware emulation or FPGA evaluation) with less features availed in the final silicon.

FEATURES

- Processor execution control
  - *Run, Halt*
  - *Reset*
  - *Step into instruction*
  - *Skip Instruction*
- Read-write all processor contents
  - *Program Counter (PC)*
  - *Program Memory*
  - *Data Memory*
  - *Special Function Registers (SFRs)*
  - *Accumulator A, B*
  - *Index registers X, Y*
  - *Condition Code Register - CCREG*
  - *Stack Pointer*
- Unlimited number of software breakpoints
  - *Program Memory*
  - *Data Memory*
  - *Special Function Registers (SFRs)*
- Hardware execution breakpoints
  - *Program Memory*
  - *Data Memory*
  - *Special Function Registers (SFRs)*
- Hardware breakpoints activated at a
  - *certain program address (PC)*
  - *certain address by any write into memory*
  - *certain address by any read from memory*
  - *certain address by write into memory a required data*
  - *certain address by read from memory a required data*
- Automatic adjustment of debug data transfer speed rate between HAD and Silicon
- Three-wire communication interface
- Fully static synchronous design with no internal tri-states

FEATURES

- Two working modes
  - *hardware emulator*
  - *software simulator*
- Source Level Debugging:
  - *C line execution*
    - *Line by line*
    - *over function*
    - *out of function*
    - *skip line*
  - *ASM code execution*
    - *Instruction by instruction*
    - *over instruction*
    - *out of function*
    - *skip instruction*
  - *ASM, C source code view*
- Symbol Explorer provides hierarchical tree view of all symbols:
  - *modules*
  - *functions*
  - *blocks*
  - *variables*
- Symbolic debug including:
  - *variables*
  - *variable type*
- Contents sensitive Watch window
- Unlimited number of software breakpoints
  - *Program Memory*
  - *Internal (direct) Data Memory (DM)*
  - *Special Function Registers (SFR)*
- Real-time hardware breakpoints
  - *Program Memory*
  - *Data Memory (DM)*
  - *Special Function Registers (SFR)*
- Set/clear software or hardware breakpoints in Assembler and C Source Code
- Load Program Memory content from:
  - *S19 HEX files*
  - *Intel HEX files*
  - *ELF/DWARF 2.0.0*
  - *IAR UBROF*
- Auto refresh of all windows
  - *Registers' A, B, CCREG, X, Y, SP, PC*
  - *Data Memory (DM)*
  - *Special Function Registers (SFR)*
  - *Timers / Counters*
  - *Compare / Capture Channels*
  - *UART – SCI*
  - *SPI*
  - *I/O Ports*
- Dedicated windows for peripherals
- Configurable auto refresh time period with 1s step resolution
- Status bar containing number of actually executed instructions, number of clock periods and real processor speed rate
- The system runs on Windows® 2000/2003/XP/7/8/8.1 (both 32 and 64 bit) PC

DEBUG SOFTWARE

The **DoCD™** Software (DS), is a Windows based application. It is fully compatible with all existing 68XX C compilers and Assemblers. The DS was designed to work in two major modes: software simulator mode and hardware debugger mode. Those two modes, allow the pre-silicon software validation in simulation mode and then, real-time debugging of developed software inside silicon - using debugger mode. Once loaded, the program may be observed in Source Window, run at full-speed, single stepped by machine or C-level instructions or stopped at any of the breakpoints and watch-points. The DoCD™ Debug Software supports all DCD's D68XX and DF68XX IP Cores with their particular configurations.

D68HC11 AND DF6811 MICROCONTROLLERS OVERVIEW

The main features of each DF68XX family member have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application. You can specify your own peripheral set (including listed above and the others) and request the core modifications.

Design	Speed acceleration	Physical Linear memory space	Paged Data Memory space	Motorola Memory Ex-pansion Logic	Interrupt sources	Interrupt levels	Real Time Interrupt	Data Pointers	READY for Prg. And Data memories	Compare\Capture	Main Timer System	SCI (UART)	I\O Ports	SPI M/S Interface	Watchdog Timer	Pulse accumulator	Interface for additional SFRs	DoCD Debugger	Size – ASIC gates
D6802	1	64k	64k	-	2	2	-	-	-	-	-	-	-	-	-	-	-	✓	3 900
D6803	1	64k	64k	-	2	2	-	-	-	-	-	-	-	-	-	-	-	✓	6 000
D6809	1	64k	64k	-			-	-	-	-	-	-	-	-	-	-	-	✓	9 000
DF6805	4.1	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	6 700
D68HC05	1.0	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	6 700
DF6808	3.2	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	8 900
D68HC08	1.0	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	8 900
D68HC11E	1.0	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓	✓	✓	✓	✓	12 000
D68HC11F	1.0	64K	64K	-	20	17	✓	1*	*	5/3*	1*	✓*	7	✓	✓	✓	✓	✓	13 500
D68HC11KW1	1.0	1M	1M	✓	25	22	✓	1*	*	13/6*	3*	✓*	10	✓	✓	✓	✓	✓	21 000
D68HC11K	1.0	1M	1M	✓	20	17	✓	1*	*	5/3*	2*	✓*	7	✓	✓	✓	✓	✓	16 000
DF6811E	4.4	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	12 000
DF6811F	4.4	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	13 000
DF6811K	4.4	1M	1M	✓	20	17	✓	1*	*	5/3*	2*	✓*	7	✓	✓	✓	✓	✓	16 000

D68HCXX family of High Performance Microcontroller Cores

+ optional | * configurable

AREA UTILIZATION

The following table gives a survey about the Debug IP Core area in the FPGA and ASIC devices.

Device vendor	Area
ALTERA	760 LC
XILINX	380 Slices
ASIC	2800 gates

FEATURES

- USB communication interface to target host at FULL speed
- Synchronous communication interface to Debug IP Core through DTAG interface
- Supports following I/O voltage standards
  - *3.3 Volt systems*
  - *2.5 Volt systems*
  - *1.8 Volt systems*
  - *1.5 Volt systems*
- Single power supply directly from USB
- Small physical dimensions

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
docddatai	input	DoCD™ data input
docddatao	output	DoCD™ data output
docdclk	output	DoCD™ clock line

PINOUT

The following pins are used by DoCD™ debug IP Core.

CONTACT

Digital Core Design Headquarters:

Wroclawska 94, 41-902 Bytom, POLAND

e-mail: info@dcd.pl
tel.: 0048 32 282 82 66
fax: 0048 32 282 74 37

Distributors:

Please check: http://dcd.pl/sales